MOSFET Gate Driver Circuit Design for High Repetitive (200kHz) High Voltage (10kV) Solid-State Pulsed-Power Modulator

Hyun-Bin Jo, Seung-Ho Song, Seung-Hee Lee, and Hong-Je Ryoo, Member, IEEE

Abstract—Solid-state pulsed power modulators can effectively generate high repetition rate pulses, which are required in applications where the process rate depends on the repetition rate, e.g., plasma source ion implantation and deposition, plasma immersion ion milling, and diamond-like carbon coating. In this study, a solid-state pulsed-power modulator for generating high repetitive pulses is developed. Active pull-down circuits and designed Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) gate drivers are applied to the modulator without increasing its size. The drivers enable a fast rise, fall time and minimize pulse width, which are effective for high-repetition-rate pulse applications. The developed modulator exhibits a maximum output pulse voltage of ±10 kV, maximum output pulse current of 50 A, pulse width between 200 ns and 10 µs, maximum pulse repetition rate of 200 kHz, and average output power of 10 kW. The operation principle of the designed MOSFET gate driver is analyzed in detail. Experimental results show that the modulator operates stably at a high repetition rate of 10 kHz and 200 kHz and the feasibility of this proposed circuit for high repetition rate operation are verified.

Index Terms—Pulsed power modulator, Gate driving Circuit, Pulse power systems, Solid-state Marx modulator

I. INTRODUCTION

The basic concept of pulsed-power generators is to discharge the energy accumulated over a relatively long time in a very short time; therefore, they can handle high peak powers. Recently, pulse power modulators based on a semiconductor switch have attracted considerable attention owing to their long life-span and high control ability [1]–[9]. However, owing to the limit of the switch rating, a series or parallel stacking method is used for high voltage and current output. The parallel and series stacking methods are mainly used in applications that require high current pulse [21] and high voltage pulse, respectively. In this study, the series stacking method is applied to a circuit for generating high voltage pulses. In applications where the process rate depends on the repetition rate, such as plasma source ion implantation and deposition, plasma immersion ion milling, and diamond-like carbon coating [10]–[13], a high pulse repetition rate (PRR) is required, which can be effectively achieved by solid-state modulator. On the other hand, modulators with various types of pull-down circuits have been proposed for effectively discharging the residual energy of reactors at turn-off to achieve a high repetition rate and output pulses with low loss since pull-down resistors are not required [14]–[18]. Furthermore, a modulator based on a power cell was developed [19]–[20]. In this modulator, if one of the multiple semiconductor switches stacked in the modulator is turned on later than the others, it generates stable pulses through the bypass diode. The repetition rate of this modulator was up to 50 kHz. However, there are limitations to generating high repetition rate pulses of several hundred kHz or more. In [19], there is no separate circuit for discharging the residual energy of the load (demonstrating the characteristics of a capacitive load) when the pulse current is extinguished. There is a limitation that increases the turn-off time of the pulse. Also, IGBTs selected as the discharging switches due to the high reliability of the arc are not suitable for generating high repetitive pulses compared to the SiC MOSFETs because of the high turn-off losses owing to the current tail of the IGBT. Further, due to the long turn-off delay time of approximately 110 ns (FGL40N120AND), there is a limit to implementing the narrow pulse width. In this study, we develop a power cell-based modulator that can generate high-repetition-rate pulses of 200 kHz based on the modulator.
developed in [19]. In addition, wide bandgap switch SiC MOSFET was used as a discharge switch, and its optimized gate driver was designed. Because this modulator uses a control loop method instead of an optical signal for pulse control, there is no need for a separate power source for isolating and driving multiple stacked switches. As a result, the volume and cost of the modulator can be minimized. In addition, despite not having to consider an external device [22] to compensate for sudden fluctuations in the source current due to the discontinuous power demand problem, this modulator has reliable input and output stability by using current source charging method and by continuously sensing and adjusting the desired charging voltage. As well as that, active pull-down circuits are applied to the solid-state modulator based on a power cell driven by a control loop. Through the optimization of the gate driver circuit, we achieve a fast fall and rise time of 30 ns, pulse width of 200 ns, and maximum PRR of 200 kHz without changing the compact structure of the existing modulator. Moreover, the reliability of the modulator is improved by designing a circuit that prevents parasitic turn-on, which is frequently caused by currents flowing through the Miller capacitor of a MOSFET. As a result, while inheriting the advantages of the existing high charging efficiency and power density, it is completed with a high repetition pulse modulator with 200 kHz repetition rate, fast rising, and falling time and active pull-down circuit.

II. OPERATION PRINCIPLE OF PROPOSED HIGH-REPETITION-RATE SOLID-STATE PULSED-POWER MODULATOR

![Circuit diagram of the proposed 10 kV solid state pulsed power modulator.](image1)

The modulator is designed for 10 kV 200 kHz repetition-rate pulses and consists of a 10 kW capacitor charger, power cell-based MOSFET stacks, on / off pulse controller, gate drivers, and control loop to supply isolated signal and power to stacked MOSFETs. The overall structure of the modulator is shown in Fig. 1. The features of the proposed modulator configuration and the proposed new gate driving circuit for high repetition driving are described in the following subsections.

A. Structure of the high-repetition-rate pulsed-power modulator with active pull-down circuit

The modulator is based on a Marx generator, which charges a storage capacitor Cs in parallel and discharges it in series and achieves high charging efficiency by charging with a current source via an LC series resonant zero-voltage-switching phase shifted PWM converter. To lower the charging voltage in a general Marx generator, a number of capacitors are charged with a relatively low voltage source that is equal to divided by the number of Marx stages from the output voltage. In this study, we charge each capacitor through a current source from multiple secondary windings by applying the modified form of a Marx generator. The voltage of the storage capacitor is continuously sensed and regulated up to the desired charging output voltage. The details of the capacitor charger can be found in [19]. The discharge section of the modulator consists of six power cells. Twelve main MOSFETs (M1 to M12) and 12 storage capacitors (Cs1 to Cs12) are connected in series to generate pulses with a maximum voltage of 10 kV.

Each storage capacitor charged in the form of a voltage doubler in each power cell has a maximum charging voltage of 833 V, which is also the maximum voltage that the two discharging MOSFETs each withstand. During pulse discharge, two discharge MOSFETs connect each storage capacitor voltage series to generate a pulse. Therefore, the pulse voltage output from the unit power cell is 1.67 kV. The advantage of a power cell system is that the voltage across the main MOSFET does not exceed that of one storage capacitor; even if a synchronization problem occurs, the switch can be protected from overvoltage because the pulse current flows through the bypass diode. One power cell has two main MOSFETs, two
by using the multi-delay within 30 ns was selected as the discharging switch. The C2M0040120D (CREE) with 1200 V rating and main switch is long, a short is replaced by a MOSFET. However, if the turn

An on/off pulse voltage generated from a pulse controller is applied to this single loop; by using an on/off pulse with a narrow pulse width, it is possible to use a small core. This helps to design a modulator with a compact structure. The core HS12 based on Mn–Zn ferrite, which has good high-frequency characteristics, was selected in the control loop to obtain a 200 kHz repetition rate. Based on equation (1), a small T16 × 10 × 6 core was selected for the compact design of the modulator while preventing the AC magnetic flux density ∆B of the transformer from exceeding the saturation magnetic flux density Bs at to avoid transformer saturation. Here, the product $\lambda$ of voltage and time applied to the transformer is 4 μ [V-s], and the cross-section Ac of the core is 15.9 [mm$^2$]. In addition, a series capacitor was connected to prevent DC saturation of the control loop transformer. Moreover, this series capacitor plays an important role in generating high repetition pulses in the control loop. To obtain a gate voltage with a short pulse width of 200 ns or less, the on pulse width is reduced to 100 ns or less. In this case, the off pulse width is increased to compensate for the insufficient energy supplied to the 24 gate drivers. However, if the off pulse width applied to the transformer increases to more than 200 ns, it will take more than 20 μs to reset the control loop off current to 0 A. With a 200 kHz repetition rate,
reset must be done within 5 µs; therefore, long reset time is a limitation to high PRR. However, while connecting a capacitor of 200 nF or more in series to the control loop, after the off voltage, the charged capacitor is discharged through the control loop, and the reset time of the off current is reduced to 3 µs or less without discharging resistor. As a result, the restriction of the control loop side during high repetition was greatly alleviated. To implement a pulse modulator with a high repetition rate and a gate driver using a high-voltage cable and a control inverter, the following conditions are required.

1) Selection of switches with good on/off characteristics (use of high efficiency SiC MOSFETs with fast switching speed and low switching loss)
2) Implementation of a control inverter for rapid current rise and fall in a gate control loop composed of a current source
3) Gate driving circuit to rapidly increase and decrease the gate driving voltage synchronously with the gate on/off signal
4) Circuit structure that can quickly discharge the energy charged in the residual charge at the load

In this study, we investigated the design of a new gate driving circuit to realize a solid-state switch-based pulse modulator with high repetition rate.

B. Proposed Gate drive circuit for high-repetition-rate pulse modulator

Figure 2 shows the proposed gate driver circuit, which consists of main and bypass drivers to drive main and bypass MOSFETs, respectively. The two drivers are connected to the secondary side of one gate transformer (Tx1) and are controlled by an on-off pulse transmitted from Tx1. The main driver uses the on/off pulse applied from Tx1 to charge the storage capacitor C1 via full-bridge rectification, and the on/off pulse is also used as a trigger signal to apply the voltage of C1 to the main MOSFET gate. The voltage charged in C1 is supplied to the main MOSFET gate from the time when the on pulse is applied until the off pulse is applied, so that a pulse width can be formed. Furthermore, the path connecting C1 and the gate-source terminal of the main MOSFET has been minimized on the PCB to achieve a fast rise time. C3 connected in parallel with the MOSFET gate resistor R3 reduces the main MOSFET’s gate capacitance and helps to implement a fast rise time. The bypass driver is designed so that the MOSFET is turned on after a certain dead time after the off pulse is applied. In addition, a circuit was designed to prevent parasitic turn-on, which frequently occurs due to the current flowing through each Miller capacitor of the MOSFET. Therefore, it is possible to avoid damage to the switch due to over current caused by a malfunction between the main and bypass MOSFETs. In the rest of this section, we describe the modes of the proposed MOSFET gate driver.

1) Mode1: Main MOSFET turn-on mode
The on-pulse voltage generated from the pulse controller is applied to each gate driver through 12 gate transformers; then, the main MOSFETs is turned on and mode 1 starts. The storage capacitor C1 is charged through an on pulse and the C1 voltage is applied to the gate of the main MOSFET as soon as the U1 PMOS switch is turned on. In the bypass driver, an on pulse is applied to the base of Q2, and a gate discharge path of the bypass MOSFET is quickly created. Accordingly, parasitic turn-on of the main MOSFET can be prevented.

2) Mode2: Main MOSFET turn-on hold mode
Mode2 starts after the on pulse applied from Tx1 ends. Because the U1 switch is turned on until the off pulse is applied from Tx1, the C1 voltage is continuously supplied to the gate of the main MOSFET. By adjusting the pulse width using small on/off pulses, the voltage-second product area applied to the transformer can be minimized, and transformer saturation can be prevented. Thus, a small transformer can be used and a compact design can be obtained. In addition, the small inductance of the small gate transformer leads to an increase in the control loop current slope, making it easy to obtain a fast rise time. In the bypass driver, Q2 remains in the on state.

3) Mode3: Main MOSFET turn-off and dead time mode.
In dead time mode, the timing to turn on the bypass MOSFET is delayed to prevent the main MOSFET and bypass MOSFET from turning on at the same time. The off pulse charges the storage capacitor C1 through the rectifier circuit, and at the same time, U2 is turned on to quickly discharge the gate charge of the main MOSFET. In the bypass driver, C4 is charged slowly but does not exceed the threshold voltage of U3; therefore, the bypass MOSFET is in the off state.

4) Mode4: Bypass MOSFET Turn-on Mode
Mode4 starts when the voltage across C4 exceeds the threshold voltage of U3. When PMOS U3 is turned on, the bypass MOSFET is also turned on at the same time. D9 is used to prevent the gate charge of the bypass MOSFET from discharging through the inverse parallel diode of U3. In the main driver, the gate charge of the main MOSFET is discharged in the same way as Mode3. This allows the current to flow through and discharge the capacitor.

5) Mode5: Bypass MOSFET turn-on hold mode
In Mode5, because there is no on/off pulse transmitted through Tx1, the gate charge of the bypass MOSFET slowly discharges through R13, which has a relatively large resistance. C4 charged in Mode4 is discharged through Tx1, C5, R12, and R9 in a series loop, and C5 is slowly charged through this loop. Here, the voltage of C5 gradually increases, but Q2 is not turned on; therefore, the bypass MOSFET remains on. In the main driver, the turn-on state of U2 is maintained for 1 µs until both the input capacitance of U2 and R7 are discharged with RC time constant, and the gate charge of the main MOSFET is continuously discharged accordingly. Finally, in Mode6, Q2 is fully turned on, and the gate
providing the input energy of the gate driver to the gate of the main MOSFET; therefore, the operation of the BJT Q1 driven by the base current reduces the effect of malfunction resulting from the effect of the electric field owing to the high dv/dt. Through the optimized voltage distribution between R1 and R2 along with the turn-on of Q1, the difference in the turn-on timing of the drain MOSFET U1 of the 12 separate gate drivers is minimized; therefore, the gate voltage among the 12 main MOSFETs is designed to have a low synchronization error of less than 5 ns.

2) Dead time circuit implementation:
When driving the main MOSFET and bypass MOSFET simultaneously with one ON/OFF signal applied through the control loop, an appropriate dead time circuit must be implemented to prevent simultaneous turn-on operation between the two devices. In Fig. 3(c), when an off-signal pulse is applied to the gate driver input, the N-MOSFET U2 rapidly discharges the gate charge of the main MOSFET such that the main MOSFET turns off immediately. At this time, the voltage of C4 slowly rises until it reaches the threshold voltage of U3, and accordingly, the turn-on time of the bypass MOSFET can be delayed.

3) Prevent parasitic turn-on operation:
By replacing the discharge switch with the SiC MOSFET and minimizing the gate synchronization error among the 12 discharge switches to less than 5 ns, a pulse with a fast rise and fall time of approximately 30 ns was generated. However, due to the increase in dv/dt, the parasitic turn-on behavior between the complementary main MOSFETs and bypass MOSFETs must be further considered. In this study, the gate-source voltage of neither the main MOSFET nor the bypass MOSFET rises above the threshold voltage (Vth) in response to the incoming charge resulting from the Miller capacitance (Cgd). This parasitic turn-on prevention circuit was implemented using switches (U2, Q2) that minimize the impedance between the gate and source in the turn-off state of the switch.

4) Compact structure integrated gate driver:
Fig. 4 (a) is the fabricated gate driving circuit, and it is implemented using a simple structure that drives two MOSFETs by sharing one toroidal core. Fig. 4 (b) shows 12 gate drivers connected through a control loop, and an insulated high voltage cable of 20 kV was used for the control loop. In addition, by attaching an insulation heat sink, two MOSFETs are shared on one heat sink. A total of 24 SiC MOSFETs are installed in the 12 gate drivers, and the width and height, including the heat sink, are implemented within the dimensions of 330 (W) mm × 130 (H) mm. Based on this, despite the addition of 12 MOSFETs and gate drivers for the circuit shown in [19], the existing power density of 385 W/L can be maintained by applying a compact driver design and a
distinctive active pull-down circuit specialized for a power cell method that does not use any optical signals and high-voltage isolation supplies.

III. EXPERIMENTAL RESULTS

Fig. 5 shows the overall experimental setup of the proposed modulator. A 6 kΩ high-voltage non-inductive resistor was used to supply the load, and the voltage was measured using a Tektronix P6015A high-voltage probe. The Yokogawa DLM2000 Series oscilloscope was used. The output side of the modulator is composed of positive (+) and negative (−) terminals. In the experiment, the negative terminal was grounded to generate positive pulses. Fig. 6 and 7 show the different results depending on whether or not the proposed circuit is used under same voltage and current test conditions, respectively. The rise time, fall time, and minimum pulse width are 60 ns, 1.3 µs, and 1.4 µs in Fig. 6, and 30 ns, 40 ns, and 200 ns in Fig. 7, respectively, indicating that the proposed circuit improves the three effective parameters by 2–30 times. Since the effects of parasitic components are greater owing to the increase in dv/dt, the modulator has been designed with a margin so that the influence of parasitic components do not damage the discharging switches. Fig. 8 (a) shows the control loop current, on/off pulse voltage, and gate voltage of the main and bypass MOSFETs obtained using the proposed gate driver.
Here, the on/off pulse voltage was measured at the gate driver input side. The on/off pulse voltage of 300 V applied from the pulse controller is divided into 12 gate driver inputs, which is a source for synchronously driving multiple switches in an isolated manner. Fig. 8 (b) shows the gate voltage at 200 kHz.

The pulse width of $V_{gs\_main}$ and $V_{gs\_bypass}$ was set to 100 and 500 ns, respectively. The 2–10 kV variable pulse amplitude waveform and 1–10 $\mu$s variable pulse width waveform shown in Fig. 9 (a) and (b), respectively, indicate that this modulator can be widely used in various application fields, not only in high-repetition applications. Fig. 10 shows the results of the 10 kV 200 kHz continuous high-repetition pulse test.

Through this experiment, the reliability and superiority of the proposed circuit were verified. Fig. 11 shows the experimental results of the synchronous driving characteristics of the discharge switch. The figure shows the gate driving signals when synchronously driving 12 main MOSFETs and 12 bypass MOSFETs and the measured jitter characteristics of the main switch gate rising pulse. From the figure, it can be seen that the designed gate driving circuit shows a high synchronization rate, and it can be confirmed that stable gate driving is possible. As for the jitter characteristics, it was confirmed that 12 switches showed a maximum synchronization error of 5 ns. Fig. 12 shows the charging voltage waveforms of 12 storage capacitors.
charged in a voltage doubler by one charging loop. Each capacitor is charged with a reference voltage of 833V, and the difference between the maximum and minimum charging voltage of each capacitor is approximately 55V, which is ±3.6% from the reference voltage. It was confirmed that it satisfies the capacitor voltage balance within 5% of the design goal.

Finally, Fig. 14 is the result of measuring the efficiency of the modulator to decrease by approximately 3% in the discharge section. Finally, Fig. 14 is the result of measuring the efficiency of this modulator as the repetition rate increases. The operating conditions are 10 kV, 10 A, and a pulse width of 500 ns, and this shows the result of measuring the charging efficiency of the capacitor charger and the switching loss of each discharge switch and the efficiency of the entire modulator as the repetition rate increases. With the increase of the pulse repetition rate, the charging efficiency increased as the capacitor charger approaches the rated operating condition, and then the maximum charging efficiency of 93% was achieved, and the switching loss increased with the increase of the pulse repetition rate; the overall efficiency was found to reach a maximum of 89% with the increase in output power and charging efficiency.

**IV. CONCLUSION**

In this study, we analyzed a 10 kV 200 kHz high repetition pulse modulator based on novel gate drivers. The modulator was composed of a combination of multiple power cells, and an active pull-down circuit and the proposed drivers were applied to the modulator. The minimum pulse width and rise and fall time, which are important for high repetition pulse applications, were shown to be significantly improved with the proposed modulator. Despite the additional circuit being applied, the modulator did not increase the size of the modulator (430 (W) mm x 150 (H) mm x 400 (D) mm) and had a high average power density of 385 W/L. Further, because the modulator did not require pull down resistors and additional cooling systems, except for the air-cooling system, pull-down losses were greatly reduced and the volume of the entire system was minimized. The switching stability was improved by implementing a circuit that prevents parasitic turn-on of the discharge MOSFET. The structure of the modulator for high-repetition-rate pulse output and the design and operation principle of the proposed gate driving circuit were analyzed in detail. In the experiment, a 10 kV 200 kHz repetition rate, 200 ns minimum pulse width, 30 ns rise time, and 40 ns fall time were achieved, and the continuous high repetition switching capability was verified. These results show that the modulator with the proposed gate driving circuit is suitable for high repetition rate applications.

**REFERENCES**


IEEE POWER ELECTRONICS REGULAR PAPER/LETTER/CORRESPONDENCE


Hyun-Bin Jo received the B.S. degree in electronic engineering from Catholic University, Bucheon, South Korea, in 2016. He is currently pursuing his M.S. and Ph.D. degrees at the Department of Energy Engineering, Chung-Ang University, Seoul. His current research interests include soft-switched resonant converter applications and high-voltage pulsed-power supply systems.

Seung-Ho Song received his B.S. degree in electrical engineering from the Kwang-Woon University, Seoul, South Korea, in 2016. He is currently pursuing his M.S. and Ph.D. degrees at the Department of Energy Engineering, Chung-Ang University, Seoul. His current research interests include soft-switched resonant converter applications and high-voltage pulsed-power supply systems.

Seung-Hee Lee received the B.S. and M.S. degrees in energy systems engineering from Chung-Ang University, Seoul, South Korea, in 2019 and 2021. Since 2021, he has been with the Korea Electrotechnology Research Institute (KERI), Ansan, South Korea, as an engineer in the High Voltage Evaluation Division. His research interest is a high voltage pulsed power generator.

Hong-Je Ryoo (M’17) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Sungkyunkwan University, Seoul, South Korea, in 1991, 1995, and 2001, respectively. From 2004 to 2005, he was a Visiting Scholar with WEMPEC, University of Wisconsin-Madison, Madison, WI, USA. From 1996 to 2015, he joined the Electric Propulsion Research Division as a Principal Research Engineer, the Korea Electrotechnology Research Institute, Changwon, South Korea, where he was a Leader with the Pulsed Power World Class Laboratory, a director of Electric Propulsion Research Center. From 2005 to 2015, he was a Professor with the Department of Energy Conversion Technology, University of Science and Technology, Deajeon, South Korea. In 2015, he joined the School of Energy Systems Engineering, Chung-Ang University, Seoul, where he is currently a Professor. His current research interests include pulsed-power systems and their applications, as well as high-power and high-voltage conversions. Prof. Ryoo is an Academic Director of the Korean Institute of Power Electronics, an International Cooperation Director of the Korean Institute of Electrical Engineers, and the Vice President of the Korean Institute of Illuminations and Electrical Installation Engineers.

Woon University, Seoul, South Korea, in 2019 and 2021. Since 2021, he has been with the Korea Electrotechnology Research Institute (KERI), Ansan, South Korea, as an engineer in the High Voltage Evaluation Division. His research interest is a high voltage pulsed power generator.