Abstract—This study presents a simplified design for a solid state pulsed power modulator (SSPPM) based on a power cell structure. Similar to the Marx generator, the power cell structure has advantages such as reliability and modularity. In addition, the proposed SSPPM includes a capacitor charger that is simple and compact. The operating principle of, and the design considerations taken for, the SSPPM are discussed from a practical viewpoint. Based on a reasonable approximation, simplified design equations are developed for a capacitor charger and a high-voltage pulse-switching part, which are comprised of an LCC resonant converter and a power stage, respectively. Accordingly, detailed design procedures are proposed to develop the SSPPM with the following specifications: 40 kV, 20 A, 300 µs, 200 Hz, and 50 kW. The experimental results verify the specifications at the rated operating condition with an efficiency of 92.4%, and also confirm reliable arc-protection performance. Finally, the proposed design methodology, which utilizes simplified equations, can be used for designing an SSPPM based on the power cell structure for extensive applications.

Index Terms—Pulse generation, pulse power supplies, resonant inverters.

I. INTRODUCTION

Currently, high-voltage pulsed power modulators based on solid-state switches are widely used in pulsed-power applications that require a relatively high repetition rate, high efficiency, low jitter, and long lifespan [1]–[19]. In particular, the solid state pulsed power modulator (SSPPM) that uses an insulated gate bipolar transistor (IGBT) and/or metal-oxide-semiconductor field-effect transistor (MOSFET) has many advantages owing to its fast switching characteristics. However, the voltage limitations of the semiconductor switches should be overcome to apply a high-voltage pulse. Accordingly, studies on SSPPMs have been reported, and various configurations, such as direct switching from a capacitor bank [1], voltage boost-up using a pulse transformer [2], vector inversion using a coupled transformer [3], and modular structure based on the Marx generator [4], are introduced. Each method that generates a high-voltage pulse has its own advantages [5].

In particular, the solid-state Marx modulator is widely used to generate a controllable rectangular pulse, as it requires a relatively low charging voltage compared to the output pulse voltage; moreover, a modular design is possible [6]–[9]. Hence, to utilize these advantages, a power cell structure is proposed to improve the performance of the SSPPM in terms of the efficiency and power density, even if it has restriction to increase maximum output pulse voltage by only adding the power cells [10]–[18]. A distinctive characteristic of the power-cell-based SSPPM is that it includes a capacitor charger for simultaneously charging multiple capacitors. Compared to the general scheme of the Marx modulator, which utilizes an external high-voltage dc source with a charging switch, the proposed circuit delivers high-frequency ac power to each cell through a multivinding transformer. Hence, the design is compact, and utilizes a minimum number of components. In addition, a soft-switching-based resonant inverter can be effectively designed by using the parasitic component of the multivinding high-voltage transformer [19]. Owing to these advantages, a power-cell-based SSPPM is proposed for various types of pulsed-power applications. However, to implement the SSPPM and achieve high performance in terms of efficiency, reliability, and power density, several technicalities need to be considered.

Based on the required specifications, this study presents a simplified guideline and equations to design and implement the power-cell-based SSPPM. The detailed components include an LCC resonant inverter for high-efficiency capacitor charging, a transformer for delivering the charging power, a power cell for applying the pulse, and a protection algorithm for reliable operation against arc generations, and are discussed in the following sections.

II. OPERATING PRINCIPLE AND DESIGN CONSIDERATIONS OF THE SSPPM BASED ON THE POWER CELL STRUCTURE

Fig. 1 shows the overall scheme of the power-cell-based SSPPM [10]–[14]. It mainly comprises a capacitor-charging part and a pulse-switching part. The capacitor-charging part includes...
Fig. 1. Overall scheme of the power-cell-based SSPPM.
a resonant inverter (S1–S4, C_s, L_n, C_p1–C_p48) and a power loop (TR_CIsolation, TR_Stage) to generate and transfer high-frequency ac charging power, respectively. The power loop, which represents the secondary winding of the TR_CIsolation, couples the resonant inverter with the power stage simultaneously. Each power stage includes a stage transformer (TR_Stage) and four power cells. Four secondary windings (n2,1–n2,4) in each power stage (e.g., Power Stage1) charge eight storage capacitors (C_{s1}–C_{s8}) through rectifier diodes (D_{s1}–D_{s8}). The voltage-doubled rectifier circuit helps to reduce the required number of secondary windings by charging two storage capacitors in each power cell. Compared to the general charging scheme of the Marx modulator, which uses a separated high-voltage dc source with additional semiconductor devices for charging [6], the proposed configuration does not require additional components for charging the storage capacitors. In addition, the design is compact because the high-voltage insulation distance for designing the charger and the pulse-switching part is considered together. On the other hand, the power loop is required to ensure isolation between the primary resonant inverter and secondary power cell. In other words, the insulation strength of the power-loop cable should be greater than the maximum pulse output voltage. Considering the required insulation strength and the high-frequency rms current, a cable with a relatively large cross-sectional area is required for the power loop. To overcome this limitation of the power-cell-based SSPPM, two solutions are suggested in this study. The first is inserting an isolation transformer (TR_CIsolation) between the resonant inverter and the power cell, which provides a second step isolation. In particular, the secondary winding of TR_CIsolation (node PPL in Fig. 1) is intentionally connected to a storage capacitor (power stage 3, power cell 3_4, node PC3_8), which has potential that is nearly half of the pulse output. This configuration, wherein the potential of the power loop is applied as half of the pulse output, can halve the required insulation strength of the power loop. Consequently, the thickness of the insulation layer can be minimized. The second method involves reducing the cross-sectional area of the conductor by decreasing the rms value of the resonant current. Hence, the resonant tank parameters should be designed to achieve less crest factor. Based on the trapezoidal approximation of the LCC resonant converter, a detailed design guideline is discussed in the following section. Furthermore, the charging voltage of the storage capacitors should be balanced to prevent over-voltage across the switches (S1–S48) and allow simple control of the charging voltage. The voltage between the capacitors inside each power cell is balanced by using equalizing resistors (R_{s1}–R_{s48}). The tertiary winding of each power stage transformer (n3) is specifically configured to compensate the voltage difference between the power stages. The tertiary windings are connected in parallel (PB1"+" ~ PB6"+", PB1"−" ~ PB6"−"), and the compensating current flows between the stages. Consequently, the charging voltage between the storage capacitors is balanced. This helps to control the pulse output voltage easily by sensing the voltage across the two storage capacitors (C_{s1} and C_{s2}) located at the ground side.

The pulse-switching part comprises a full-bridge inverter (S5–S8), a control loop (TR_PIsolation, TR_GD), and semiconductor switches (Sw1–Sw48, Sw1’–Sw48’) with their drive circuits (GD for Sw1&Sw48, Sw1’&Sw48’). To control the pulse width (PW) and pulse repetition rate (PRR), the full-bridge inverter and control loop are designed to generate and transfer the on/off pulse, respectively. The pulse-control algorithm is known from the waveform of the on/off pulse (V_{off/on}(t)) and the gate–emitter voltage (V_{GE}(t)), as shown in Fig. 2. The gate drive circuit (GD) for pulse-switching IGBTs (Sw1~Sw48) is designed to provide and maintain V_{GE}(t) when it receives the “on” pulse from control loop. In addition, V_{GE}(t) starts to decrease when the “off” pulse is applied. Controlling V_{GE}(t) by means of the bipolar short pulse allows for the size of TR_PIsolation and TR_GDs to be reduced. Accordingly, the PW and PRR are controlled based on the time delay between the on and off pulses and the time delay between the on and on pulses, respectively [10]. The function of the pulse isolation transformer (TR_PIsolation) is similar to that of the TR_CIsolation. Therefore, a node referred to as PCL1"+" is connected to a storage capacitor that has almost half of the potential of the output pulse (node PC3_8). A high-voltage insulated cable couples the control loop with eight gate drivers (GDs) inside each power stage. To combine the control loop between the stages, a parallel configuration (PCL1"+" ~ PCL6"+", PCL1"−" ~ PCL6"−") is employed, because the input voltage of the full-bridge inverter (V_{dp}) is limited. With the help of the simple gate-driving operating concept, an arc protection algorithm is proposed using two additional off pulses, as shown in Fig. 2. When the pulse-output current sensor detects an arc, the on/off pulse controller generates the “off” pulse to pull down the gate voltage of the semiconductor switches. In addition, the second “off” pulse helps to confirm that the performance of the arc protection circuit is reliable. Compared to the arc protection circuit implemented in each GD circuit, the proposed protection circuit has advantages such as simplicity in design, because of its minimized number of components, and flexibility in choosing a suitable arc-current level [12]–[14]. Furthermore, the proposed GD is designed to drive not only the switches (Sw1~Sw48) that apply the pulse to the load, but also the switches (Sw1’~Sw48’) that pull down the output pulse. Compared to a conventional power cell structure comprising a switch with a bypass diode [11]–[14], a controllable semiconductor called the bypass switch (Sw1’~Sw48’) is used in the proposed SSPPM instead of the bypass diode [10]. The antiparallel diode of the bypass switch can serve as the bypass diode. In addition, the bypass switch helps to discharge the energy.

![Fig. 2. Waveforms of on/off pulse and gate-emitter voltage.](image-url)
stored in the parasitic capacitance and decrease the falling time without an additional pull-down resistor. The circuit shown in Fig. 1 is intentionally drawn with node numbering, PP1_1–PP6_8, without connection because the proposed SSPPM facilitates the configuration for both the positive and negative pulse outputs.

As depicted in Fig. 3, the following are the node connections for both polarities.

1) Node connection for the positive output pulse
   Ground → PP1_8, PP1_7 → PP1_6, PP1_5 → PP1_4, PP1_3 → PP1_2, PP1_1 → PP2_8, ..., PP6_3 → PP6_2, PP6_1 → + Output.

2) Node connection for the negative output pulse
   Ground → PP1_1, PP1_2 → PP1_3, PP1_4 → PP1_5, PP1_6 → PP1_7, PP1_8 → PP2_1, ..., PP6_6 → PP6_7, PP6_8 → − Output.

To change the output pulse polarity, it is necessary to change the connection between the power stages but modifying the connection in each power stage is not required.

III. Detailed Design of SSPPM

Depending on the required specifications of the SSPPM summarized in Table I, the detailed design procedures are described in this section.

A. Design of Capacitor Charger Based on Trapezoidal Approximation of LCC Resonant Converter

The simplified circuit of the capacitor-charging part, shown in Fig. 1, is illustrated in Fig. 4. The power stage transformers (TR_Stage1–TR_Stage6), parallel resonant capacitors (C_p1–C_p18), and storage capacitors (C_s1–C_s48) are equalized as TR_eq, Cpeq, and C_seq, respectively.

To understand the capacitor charger based on the LCC resonant converter, the detailed design is explained by using an equivalent parallel resonant capacitor (C_p) placed on the primary side of the transformer. It should be noted that the parallel resonant capacitors are practically implemented in parallel with the rectifier diodes. Hence, the leakage inductance of the transformers (TR_CIsolation and TR_Stage) can be employed for the resonant inductor by using this configuration. Furthermore, the parallel resonant capacitor can be effectively used to balance the voltage of the rectifier diodes when the diodes are stacked in series [22]. Considering the major operating waveforms and the equivalent circuit shown in Fig. 5, the detailed design of the capacitor charger is as follows.

1) Brief Explanation About Trapezoidal Approximation of the LCC Resonant Converter: The operating principle and analysis of the LCC resonant converter is well known and the detailed design procedures are introduced previously [20], [21]. This study focuses on the simplified design of the LCC resonant converter to reduce the rms value of the resonant current based on the trapezoidal approximation. For a trapezoidal shape of the resonant current, the value of the series resonant capacitor (C_s) should be considerably greater than C_p. In addition, the voltage across the series resonant tank (L_s, C_s) during Mode2&4 (M2&M4) should be reduced to maintain the resonant current as an almost constant value. Accordingly, the resonant current increases abruptly and stabilizes during M1 and M2, respectively, owing to the above two design assumptions.

<table>
<thead>
<tr>
<th>TABLE I Design Specifications of SSPPM</th>
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<tbody>
<tr>
<td>AC input voltage, V_ac</td>
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<tr>
<td>DC input of the capacitor charger, V_dc</td>
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<tr>
<td>DC input of the on/off pulse generator, V_if</td>
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<tr>
<td>Maximum pulse output voltage, V_pulse, max</td>
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<td>Maximum pulse output current, I_pulse, max</td>
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<td>Maximum pulse repetition rate, PRR_max</td>
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<td>Maximum pulse voltage droop rate, V_droop rate</td>
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<tr>
<td>Maximum charging power, P_o, max</td>
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</table>

Fig. 3. Node connection diagram for positive and negative pulse output.

Fig. 4. Simplified circuit of capacitor charger based on LCC resonant converter.
2) Calculation of Transformer Turns Ratio: The turns ratio of the equivalent transformer, $1 : N_{eq}$, should be calculated such that the voltage across the series resonant tank during M2 and M4 is minimum. Accordingly, the turns ratio of $T_{req}$ is calculated by equating $V_{dc}$ and $V_{pri}$, as in (1). An input voltage of 513 V is considered in the calculation because the resonant current value at $t_2$ increases and decreases slightly, depending on the high and low input voltage conditions, respectively

$$N_{eq} = \frac{V_{sec}}{V_{pri}} = \frac{\frac{1}{2} V_{dc,\max}}{V_{dc}} \cdot \frac{1}{2} \approx 40. \quad (1)$$

3) Determining the Peak Value of the Resonant Current ($I_{Ls,peak}$) and Frequency Ratio ($f_{s,\min} / f_{op}$): The required value of the peak resonant current ($I_{Ls,peak}$) that provides a maximum charging power ($P_{o,max}$) of 50 kW should be determined to calculate the resonant tank parameters. Based on the ampere–second area (charge $Q$) of the resonant current, the design equations for the $LCC$ resonant converter are introduced [20]. Based on the proposed equations, the relationship between $P_{o,max}$ and $I_{Ls,peak}$ is simplified by assuming a trapezoidal shape of the resonant current, as in (2). This equation helps to design the $LCC$ resonant converter efficiently, despite having been derived by neglecting the effects of Q1’ and Q2’, shown in Fig. 5. It should be noted that this equation is valid only in a limited switching-frequency range, because the switching frequency should be less than 1.6 times the parallel resonant frequency ($f_{op}$: resonant frequency calculated using $L_s$ and $C_p$)

$$P_o = V_{dc} \times I_{Ls,peak} \times \left(1 - \frac{5}{8} \cdot \frac{f_s}{f_{op}}\right). \quad (2)$$

By equating (2) and the dc input power ($V_{dc} \cdot I_{dc}$), the current ratio of the required $I_{Ls,peak}$ to the ideal $I_{dc}$ can be drawn with different frequency ratios of the minimum switching frequency ($f_{s,\min}$) to the parallel resonant frequency ($f_{op}$).

The solid line in Fig. 6 indicates that a low value of the frequency ratio ($f_{s,\min} / f_{op}$) helps to reduce the required $I_{Ls,peak}$ for the rated operation. This is because the high parallel resonant frequency reduces the circulating energy during M1 and M4. On the other hand, the circulating energy is closely related to the light load operation of the $LCC$ resonant converter. The dashed line in Fig. 3 indicates the power ratio of the output power at three times $f_{s,\min}$ ($P_{o,3f_{s,\min}}$) to the maximum output power at the minimum switching frequency ($P_{o,max}$). The result clearly shows the difficulty in operating at the light-load condition based on the increase in the frequency ratio. This tradeoff between the required $I_{Ls,peak}$ and the light-load operation characteristic need to be considered based on the type of application.

For example, a capacitor charger that requires charging without regulation can be designed with a low frequency ratio. In contrast, if the dc power supply and/or the capacitor charger for a SSPPM require output voltage regulation, the operating switching-frequency range for light load operation should be considered. To design the charger for the SSPPM, a frequency ratio of 0.5 is selected such that $I_{Ls,peak}$ is less than 1.5 times $I_{dc}$, and $P_{o,3f_{s,\min}}$ is less than 10% of the rated power.

4) Determining the Maximum Voltage Across the Series Resonant Capacitor ($V_{Cs,peak}$): To validate the trapezoidal approximation, the capacitance of the series resonant capacitor ($C_s$) should be much greater than that of the parallel resonant capacitor ($C_p$). Accordingly, the abrupt increase in the resonant current during M1 and the flat waveform of the resonant current during M2 can be achieved using the parallel resonant frequency ($f_{op}$) and the series resonant frequency ($f_{on}$: resonant frequency calculated using $L_s$ and $C_s$), respectively. This relationship implies that the lower the maximum charging voltage ($V_{Cs,peak}$) of $C_s$ is, the lower rms value of the resonant current (with the trapezoidal waveform) will be. Hence, the value, $V_{Cs,peak}$, is...
determined to be a quarter of the input voltage \( (1/4) \cdot V_{dc} \). This is because \( V_{dc} \) represents the maximum charging voltage of \( C_p \) and a reasonable capacitance of \( C_s \) can be selected.

5) Calculation of the Design Parameters for Capacitor Charger: To calculate the resonant tank parameters, the minimum switching frequency \( (f_{s,\text{min}}) \) should be determined based on the power losses in S1–S4. To generate 50 kW of the maximum charging power from a single phase, full-bridge LCC resonant inverter, considerable conduction loss on the inverter switches is inevitable even if the proposed design provides less rms value of the resonant current with the trapezoidal waveform. In addition, the proposed LCC resonant converter operation has turn-off switching loss that is proportional to the switching frequency. To achieve high-efficiency, a minimum switching frequency of 30 kHz is selected based on the characteristic of power MOSFET (CAS300M12BM2, CREE) that is used for S1–S4. Accordingly, the range of switching frequencies is determined from 30–180 kHz for regulating the output from 100% to 1% load conditions, respectively. Depending on an \( f_{s,\text{min}} \) of 30 kHz, the resonant tank parameters are calculated by using (3)–(6).

From the operating waveforms of the proposed LCC resonant converter shown in Fig. 5, it is clear that the value of \( I_{Ls,\text{peak}} \) is determined during M1. Based on the equivalent circuit for M1 in Fig. 5, \( I_{Ls,\text{peak}} \) can be calculated from the sum of voltage across \( L_s \) (as numerator term: \( V_{dc} - V_{CS}(t_0) - V_{CS}(t_0) \)) and the characteristic impedance of resonant tank (as denominator term) [20]. The value of two resonator capacitor voltages \( (V_{CS}(t_0), V_{CS}(t_0)) \) is already determined, as depicted in Fig. 5. One approximation used to derive a simplified (3) is that the value of \( C_s \) does not significantly affect the resonance, and it can be ignored when calculating the value of the characteristic impedance \( Z_{op} = \frac{2 \cdot V_{dc} + V_{CS,\text{peak}}}{I_{Ls,\text{peak}}} \approx 7.94 [\Omega] \).

The parallel resonant frequency is previously found to be 60 kHz after determining the frequency ratio \( (f_{s,\text{min}}/f_{op}) \) and \( f_{s,\text{min}} \). From \( f_{op} \) and \( Z_{op} \), the resonant inductance \( (L_s) \) and the parallel resonant capacitance \( (C_p) \) are calculated by using the following:

\[
L_s = \frac{Z_{op}}{2\pi f_{op}} \approx 21.06 [\mu H] \quad (4)
\]

\[
C_p = \frac{L_s}{Z_{op}} \approx 0.334 [\mu H]. \quad (5)
\]

As shown in Fig. 5, the voltage waveform of \( C_s \) is a linear function of time owing to the almost constant value of the resonant current, and the value of \( C_s \) is calculated as (6).

Based on the analysis of the LCC resonant converter introduced in [20], the equation for \( t_{M2} \) can be simplified based on the trapezoidal approximation that ignores Q1' and Q2' in Fig. 5. The amp–second area (Q1, Q2, Q3) of the resonant current shown in Fig. 5 determines the power from input \( P_{in} = V_{dc} \times (Q1 + Q2 - Q3) \times 2f_s \) and the power transferred by transformer \( P_{T,\text{req}} = V_{dc} \times (Q2 + Q3) \times 2f_s \). From the assumption of 100% efficiency, the value of these two power terms should be the same. Accordingly, the relationship between Q2 and Q3 can be determined as \( Q1 = 2 \cdot Q3 \) that represents \( t_{M1} \) is the half of \( t_{M1} (= T_{op}/4) \). Therefore, the expression for \( t_{M2} \) can be derived as

\[
C_s = \frac{I_{Ls,\text{peak}} \times t_{M2}}{2 \cdot V_{CS,\text{peak}}} = \frac{I_{Ls,\text{peak}} \times \left( \frac{T_s}{2} - \frac{3}{8} T_{op} \right)}{2 \cdot V_{CS,\text{peak}}} \approx 5.91 [\mu F]. \quad (6)
\]

The values of the lossless snubber capacitors \( (C1–C4) \), which can be used to reduce the turn-off switching loss of the switches (S1–S4), are selected by considering the switching-frequency range and operating-load condition. To obtain wide controllable output voltages and load ranges, a MOSFET output capacitance of 2 nF is used as a lossless snubber instead of additional capacitors. The equivalent storage capacitor \( (C_{eq}) \) can serve as a filter capacitor from a capacitor-charger viewpoint, as shown in Fig. 4. On the other hand, the value of \( C_{eq} \) should be determined using the required voltage droop. The calculation steps are discussed in the following section.

B. Design of Pulse-Switching Part Including Power Stage

Based on the specifications related to the output pulse summarized in Table I, the step-by-step design procedure for the pulse-switching part is as follows.

1) Determining the Number of Power Stages \( (N_{\text{stage}}) \): The number of power stages \( (N_{\text{stage}}) \) largely depends on the core for the TR_Stage. Because the power delivered using the transformer is limited, a multistage structure is required, as shown in Fig. 1. Hence, the core should be selected to determine \( N_{\text{stage}} \). First, the required size of the core can be determined by calculating the required area product (AP) of the core as follows [23]:

\[
AP = A_W \cdot A_E = \left( \frac{P_{o,\text{max}}}{K \times \Delta B \times f_{s,\text{min}}} \right)^{4/3} \approx 1140 [cm^4]. \quad (7)
\]

To transfer the maximum charging power \( (P_{o,\text{max}}) \), the AP is calculated to be approximately 1140 cm\(^4\). The values of \( K \) and \( \Delta B \) are 0.017 (full bridge) and 0.5 T (considering the core loss of the ferrite PC40 material), respectively. From the commercialized large-size ferrite core, a PQ 107 \times 87 \times 70 core with an AP of 220 cm\(^4\) is selected, and six power stages \( (N_{\text{stage}} = 6) \) are configured to satisfy the required AP of 1140 cm\(^4\). Moreover, the multistage structure helps to design the winding structure by considering insulation between the windings.

2) Calculating the Primary Winding Turns of TR_Stage \( (N_1) \): As shown in Fig. 1, the power loop, which represents the primary windings of the TR_Stage, simultaneously couples the cores from TR_Stage1 to TR_Stage6. Based on Faraday’s law, the required \( N_1 \) for achieving the desired \( \Delta B \) (0.5 T) can be calculated using \( N_1 = A_{E} \times A_{W} \times 6 \) of the cross-sectional area of the magnetic core, where \( A_{E} \) (14.28 cm\(^2\)) is the effective cross-sectional area of the PQ 107 \times 87 \times 70 core. Accordingly, two
turns of the power loop \((N_1 = 2)\) are calculated as

\[
N_1 = \frac{V_{dc}}{\Delta B \times N_{stage} \times A_E \times 2 \times f_{x_{min}}} \approx 2 \text{ [turns]}. \tag{8}
\]

3) Determining the Number of Power Cells \((N_{cell})\): The number of power cells \((N_{cell})\) depends on the charging voltage of each cell; moreover, it is closely associated with the voltage ratings of the semiconductor switches (Sw1–Sw48, Sw1’–Sw48’). In particular, the dynamic characteristic of Sw1–Sw48 largely determines the rising time of the output pulse and the losses of pulse-switching part. Generally, the lower the ratings of the semiconductor switches, the better the dynamic performance. In addition, other considerations for selecting the semiconductor switch are the pulsed current capability and/or performance. In addition, other considerations for selecting the semiconductor switch are the pulsed current capability and/or performance. In addition, other considerations for selecting the semiconductor switch are the pulsed current capability and/or performance. In addition, other considerations for selecting the semiconductor switch are the pulsed current capability and/or performance. In addition, other considerations for selecting the semiconductor switch are the pulsed current capability and/or performance.

4) Calculating the Secondary Winding Turns of TR_Stage \((N_2)\): As shown in Fig. 1, \(N_2\) is the sum of the four secondary windings \((n2_1\text{--}n2_4)\), and it can be easily calculated by multiplying the number of primary turns, \(N_1\), and the equivalent transformer ratio, \(N_{eq}\). Thus, the number of turns for each secondary winding in the power stage is calculated as

\[
n2_1\text{--}n2_4 = \frac{N_1 \times N_{eq} \times N_{stage}}{N_{cell}} \approx 20. \tag{10}
\]

5) Determining the Value of Storage Capacitors \((C_{s1}\text{--}C_{s48})\): In addition to reducing the ripple in the charging voltage in terms of the capacitor charger, the main function of the storage capacitor is to maintain the output pulse voltage with less voltage droop. Similar to the Marx generator, the storage capacitors are configured in series to apply the high-voltage pulse. In other words, the capacitance that is calculated from the series connection of all the storage capacitors determines the maximum voltage droop rate \((\Delta V_{Droop,rate})\), depending on the values of the maximum pulse current \((I_{pulse,max})\) and PW \((PW_{max})\). When all the storage capacitors are connected in series, the value of equivalent capacitance can be calculated as \(C_{s1/2} \times N_{cell} = C_{s2} = C_{s3} = \cdots = C_{s48}\). Therefore, the value of each storage capacitance should be greater than the calculated capacitance from the desired voltage droop \((\Delta V_{Droop} = V_{pulse,max} \times V_{Droop,rate})\). Hence, the required capacitance of the storage capacitors can be calculated by using (11), which is determined to be 390 \(\mu\)F

\[
C_{s_{1}\text{--}s_{48}} \geq \frac{I_{pulse,max} \times PW_{max}}{V_{pulse,max} \times V_{Droop,rate}} \times 2 \times N_{cell} \approx 288 \text{ [\(\mu\)F]}. \tag{11}
\]

6) Calculating the Capacitance of the Practical Parallel Resonant Capacitors \((C_{p_{1}\text{--}p_{48}})\) from \(C_p\): The equivalent parallel resonant capacitor \((C_p)\) is employed to design the resonant inverter. However, for practical implementation, the parallel resonant capacitor is better implemented on the secondary side of the transformer. This is because the leakage inductance can be used for the series resonant inductor. Hence, the parallel resonant capacitor is implemented using \(C_{p_{1}\text{--}p_{48}}\), as shown in Fig. 1. Moreover, the capacitors \(C_{p_{1}\text{--}p_{48}}\) are not connected in parallel, or series with the secondary winding; however, they are connected in parallel with the rectifier diodes \((D_{r_{1}\text{--}r_{48}})\). This is because each diode in the voltage-doubled rectifier is practically implemented with two in series and is required to balance the voltage between the series stacked diodes. By connecting the parallel resonant capacitor in parallel with each diode, the capacitor can be balanced without additional components. By employing the calculated \(C_p\), the equivalent parallel resonant capacitor \((C_{p_{eq}})\), shown in Fig. 4, can be determined by dividing \(2 \cdot N_{eq}^2\) [22]. By using (12), the capacitance of each parallel resonant capacitor \((C_{p_{1}\text{--}p_{48}})\) is found to be 2.5 \(nF\)

\[
C_{p_{1}\text{--}p_{48}} = \frac{C_p}{2 \cdot N_{eq}^2} \times N_{cell} \approx 2.5 \text{ [nF]}. \tag{12}
\]

7) Determining the Value of Equalizing Resistors \((R_{r_{1}\text{--}r_{48}})\): To determine the resistance of the equalizing resistors, the voltage between the storage capacitors in each power stage should be balanced. Although a more accurate balancing is possible using equalizing resistors with lower resistance, the power loss of the resistors should be considered. By employing (13), which is used to calculate the total power loss of the resistors, the resistance of each resistor \(R_{r_{1}\text{--}r_{48}}\) is determined to be 540 k\(\Omega\) for a power loss of 0.125% compared to \(P_{o,max}\)

\[
P_{Re,loss} = \frac{V_{pulse,max}^2}{2 \cdot N_{cell} \times Re} \text{ [W]}. \tag{13}
\]

8) Design of Arc Protection Circuit: As part of the research discussed in this study, a previous study related to the GD circuit is introduced and includes a detailed operation principle [10]. Based on the proposed gate-driving concept that employs the “on” and “off” pulses for charging and discharging the gate voltage \((V_{GE})\), the arc protection algorithm is proposed using an additional “off” pulse. The controller used for generating the gate pulses in S5–S8 is designed to provide two additional “off” pulses when the arc is detected. This method is more reliable than increasing the PW of the off pulse. The design prevents the saturation of the TR_GD without increasing the cross section of the core. In addition, the arc protection level can be adjusted, unlike the conventional method that employs a protection circuit for all the drive circuits. Hence, a simple configuration and reliable operation are achieved by using the proposed arc-protection algorithm.
9) Determining the Tertiary Winding Turns of TR\_Stage ($N_3$): Ahn et al. [11] show the details of the tertiary winding with detection and protection methodologies against voltage unbalancing. For the tertiary winding, the number of turns is not a critical design factor, despite the fact that a more accurate balancing can be achieved between the stages by using a larger number of turns. This is because the compensating current will flow independently, regardless of the number of turns, and the value of the current is expected to be relatively small. However, the important design consideration is that the tertiary winding should be wound to allow better coupling with the secondary winding, in order to reflect the voltage accurately. In addition, the parallel configuration of the windings in each stage transformer is better than the winding structure introduced in [11]. This is because the effect of the leakage inductance can be reduced. Another consideration is that the insulation strength of the tertiary winding cable should be the same as that of the cable for the power loop. Based on the aforementioned considerations, one turn of the tertiary winding is determined because of the restricted area for winding, and the detailed winding structure is described in Section IV.

IV. Experimental Results of Developed SSPPM

Fig. 7 shows the overall structure and an image of the developed SSPPM. The top view of the developed SSPPM shows the detailed design structure of power stage six, including TR\_Stage6, TR\_GD, $C_p$, and $D_r$. The structure can be correlated with the circuit shown in Fig. 1. To implement the power loop, three high-voltage insulated wires are used in parallel to secure 20 kV of insulation and allow the rated rms of the resonant current. The secondary windings are wound on a specially designed bobbin, and two sections are arranged for each secondary winding. The bobbin structure provides effective insulation between the secondary windings. One turn of a tertiary winding is inserted at the center of TR\_Stage6, as shown in Fig. 7. The distance between the windings is equal owing to the structural design of TR\_Stage, and the charging voltage is balanced owing to the full winding area, along with the reduction in the difference between leakage inductances. One turn of the control loop is designed to penetrate the toroidal cores (TR\_GD), which deliver the on/off pulse to each GD circuit, which drive the switches (Sw & Sw’) simultaneously.

$D_{r48}$ and $C_{p48}$ in Fig. 7 show that the diodes ($D_{r1}$–$D_{r48}$) and the parallel resonant capacitors ($C_{p1}$–$C_{p18}$) are practically implemented as two stacked diodes, and the voltage between the two stacked diodes is balanced using the parallel resonant capacitor. To satisfy the capacitance and voltage rating of the storage capacitor, four capacitors are installed: two in series and two in parallel. The same can be observed in $C_{s41}$. Utilizing the aforementioned structure of each power stage, six power stages are configured as shown in the side view of Fig. 7.

The power loop couples the stage transformers with the resonant inverter, which is located at the bottom of the developed SSPPM. Except for the power stages, the bottom case is designed to include all the parts, such as two full-bridge inverters, two isolation transformers (TR\_C\_Isolation, TR\_P\_Isolation), an input rectifier with a filter, and a controller.

To verify the design described in this study, the developed SSPPM, shown in Fig. 7, was tested using a resistor load of 2 kΩ. The maximum pulse voltage (40 kV) and current (20 A) at the maximum PRR (200 Hz) are measured as shown in Fig. 8. With a PW of 300 μs, a voltage droop rate below 2.5% is confirmed for a pulse current of 20 A. In the operating condition, shown
in Fig. 8, the average output power is measured to be 49.57 kW. Accordingly, a maximum efficiency of 92.4% was determined by using the measured input power of 53.66 kW obtained from the ac input (Vac in Fig. 1).

Fig. 9 shows the curve of the measured efficiency versus average output power. The measured efficiency was calculated by employing not only the pulse-switching part, but also the capacitor charger.

In contrast to the direct switching method that requires RDC snubber [24], the proposed SSPPM removes the passive components for voltage balancing and features high efficiency as depicted in Fig. 9. Compared to the other solid-state Marx circuits [25]–[26] and the pulsed modulator using a pulse transformer [27], 92.4% of the maximum efficiency that was achieved based on the proposed design is relatively high. However, it should be noted that a direct efficiency comparison is not reasonable because of the different input and output specifications. The performance of the proposed arc-protection algorithm is experimentally verified as shown in Fig. 10. During the normal operating condition at 40 kV, as shown in Fig. 7(a), an external arc is intentionally generated by placing the ground wire at the high-voltage output. The arc protection waveforms, shown in Fig. 7(b), show that the pulse current gradually increases to 350 A for a duration of 2 μs after generating the arc, and subsequently, decreases after applying the “off” pulse. Accordingly, the semiconductor switches are protected against the arc. Even if the switches (Sw1–Sw48) are expected to turn off after the first “off” pulse, the operation is reliable owing to the second “off” pulse.

V. CONCLUSION

This study described a simplified design of the SSPPM based on a power cell structure. Based on the operating principle and practical design considerations, the sequential design procedures using simple equations were explained and employed to design the SSPPM with the following specifications: 40 kV, 20 A, 300 μs, 200 Hz, and 50 kW. Finally, the experimental results verify the proposed design guideline and demonstrate the high performance of the developed SSPPM in terms of high efficiency and high reliability. In the future, the developed SSPPM will be applied to radar applications that require a voltage droop below 0.5%. To satisfy the critical droop specification, an active droop compensator was being developed to be combined with the proposed SSPPM to achieve high power density without increasing the capacitance of the storage capacitors.

REFERENCES


